



Elma User Manuals: JetKit-3010

BACKPLANES

CHASSIS PLATFORMS

EMBEDDED BOARDS

EMBEDDED COMPUTING SOLUTIONS

POWER SOLUTIONS

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Revision History

Revision	Description	Date	By
1.00	Initial release	2022-08-04	FF

Preface

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1 Introduction

1.1 Symbols Explanation

	This symbol indicates danger of injury for user or risk of damage to product or components.
	This symbol indicates danger for electronic components, which can be damaged or destroyed by discharge of electrostatic electricity.
	This symbol indicates information to specific product configuration or settings of hardware.

1.2 Electrostatic Discharge (ESD)



This product includes high sensitive microcontrollers and semiconductor products that can be damaged by electrostatic discharge (ESD).

Electrostatic discharge can destroy static-sensitive devices or micro-circuitries. Damage due to inappropriate handling is not covered by the warranty.

The following precautions must be taken:

- Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.
- Pay attention to a good grounding of persons, the workstation and devices around the system, tools and packaging.
- Transport the system or other electrostatic sensitive parts in a static safe container (box or bag).
- Keep the parts in their container until the workspace around is ESD-safe.
- Use a conductive wrist strap attached to a good earth ground.
- Use anti-static mats on all surfaces in the workspace

2 Hardware

2.1 Overview

The Elma JetKit-3010 is based on the NVIDIA® Jetson AGX Xavier™ Industrial System-on-Module. It provides the ability to integrate the NVIDIA® Jetson AGX Xavier™ seamlessly into existing CompactPCI Serial infrastructure. With its industry leading performance, power efficiency, integrated deep learning capabilities and rich I/O, the NVIDIA® Jetson AGX Xavier™ enables emerging technologies with compute-intensive requirements. Designed for applications converging on artificial intelligence (AI), computer vision (CV) and advanced graphics, the AGX Xavier™ is ideal for (but not limited to): Intelligent Video Analytics (IVA), Robotics, Virtual Reality (VR), Augmented Reality (AR), Portable Medical Devices and autonomous driving.

2.2 NVIDIA® Xavier™ Software

Intentionally, the design of the JetKit-3010 was oriented on the design of the NVIDIA® AGX Xavier™ Developer Kit. This allows Software reutilization between platforms. Main differences (influencing the Device Tree) are leaving out the audio codec and usage of a different USB type C power delivery controller. The modified device tree file can be provided on request. For more information on the NVIDIA® Xavier™ module, please consult the NVIDIA® online documentation:

Jetson™ Download Center:

<https://developer.nvidia.com/embedded/downloads>

NVIDIA® Jetson™ Linux Developer Guide:

<https://docs.nvidia.com/jetson/l4t/>

Getting Started:

<https://developer.nvidia.com/embedded/learn/getting-started-jetson>

2.3 Technical Specification

The Elma JetKit-3010 is based on the NVIDIA® AGX Xavier™ Industrial module and inherits the module's features. The module adds further functionality and extendibility as well as it adapts the interface to the CompactPCI Serial infrastructure. The technical specification of the JetKit-3010 can be found in Table 1.

Table 1 - Technical Specification

Features		Specifications
SoC	GPU	Volta GPU Tensor Cores End-to-end lossless compression Tile Caching OpenGL® 4.6 OpenGL ES 3.2 Vulkan™ 1.0 CUDA® 10
	CPU	Carmel CPU Complex ARMv8.2 (64-bit) heterogeneous multi-processing (HMP) CPU Architecture Dual-core CPU clusters connected by a high-performance system coherency interconnect fabric L3 Cache: 4MB (shared across all clusters) NVIDIA® Carmel (Dual-Core) Processor: L1 Cache: 128KB L1 instruction cache (I-cache) per core; 64KB L1 data cache (D-cache) per core L2 Unified Cache: 2MB per cluster

Features		Specifications
Memory	Main Memory	256-bit DRAM interface Secure External Memory Access Using TrustZone Technology System MMU Memory Type: LPDDR4x Memory Size: 32GB
	Storage	eMMC 5.1 Flash Storage Bus Width: 8-bit Maximum Bus Frequency: 200MHz (HS400) Storage Capacity: 64GB
	Memory Slot	M.2 Slot size 2242 Socket 3 Type M PCIe x4 interface
Multimedia	Display Controller	1x HDMI 2.0a/b (up to 6Gbps)
	Multi-Stream HD Video & JPEG	Video Encode: Standards Supported: H.265 (HEVC), H.264, VP9 Video Decode: Standards Supported: H.265 (HEVC), H.264, VP9, VP8, MPEG-4, MPEG-2, VC-1 JPEG (Decode & Encode)
	Audio Subsystem	Dedicated programmable audio processor ARM Cortex A9 with NEON 2x I and Q baseband data channels Industry-standard High Definition Audio (HDA) controller provides a multi-channel audio path to the HDMI interface.
Interfaces	CompactPCI Serial	CompactPCI Serial Interface: - Compliant with PICMG® CPCI-S.0 R1.0 CompactPCI® Serial - Support for the following interfaces: - o 1x PCI Express 3.0 x8 - o 1x Gigabit Ethernet - o 1x USB3.0/2.0 (optional) - 12V Power Supply - Operation in system slot and in peripheral slot
	USB	2x USB Type C: - USB 3.1 / 2.0 - USB Type C Power: max. 5V, 3A - USB Device Mode for Programming (USB-C 1) 1x USB Type A: - USB 2.0 - USB Type A Power: max. 5V, 0.5A 1x MicroUSB (client) - Quad interface client chip - o 1x I2C Interface - o 1x JTAG Interface - o 1x UART for BMC - o 1x UART for NVIDIA® Xavier™
	Ethernet	1x RJ45 connector - 10/100/1000Mbit/s operation - Intel i210-AT Ethernet NIC - Integrated LEDs for LINK/ACT and Gigabit Ethernet Indication
	MiniHDMI	1x HDMI 2.0a/b (up to 6Gbps) via MiniHDMI connector
	MicroSD / UFS	1x MicroSD / UFS card slot
	Buttons	1x Reset Button, 1x Recovery Button
	LEDs	1x Power LED, 3x User LEDs

Features		Specifications
Interfaces	Extension Interface	1x High-Speed Mezzanine Header: - 1x PCIe x4 - 1x PCIe x2 - 1x USB2.0 - 4x CSI Camera Interfaces - Utility signals - Power
	Environmental	Operating Temperature: -20°C to +50°C (@40W power profile) Storage Temperature: -20 to +85°C
Board	Management	Integrated BMC controller handles reset management, power and voltage monitoring

2.4 Features¹

2.4.1 Volta GPU

The same Volta GPU architecture that powers NVIDIA® high-performance computing (HPC) products was adapted for use in Jetson AGX Xavier™ series modules. The Volta architecture features a new Streaming Multiprocessor (SM) optimized for deep learning. The new Volta SM is far more energy efficient than the previous generations enabling major performance boosts in the same power envelope. The Volta SM includes:

- New programmable Tensor Cores purpose-built for INT8/FP16/FP32 deep learning tensor operations; IMMA and HMMA instructions accelerate integer and mixed-precision matrix-multiply-and-accumulate operations.
- Enhanced L1 data cache for higher performance and lower latency.
- Streamlined instruction set for simpler decoding and reduced instruction latencies.
- Higher clocks and higher power efficiency.

The Volta architecture also incorporates a new generation of its memory subsystem and enhanced unified memory and address translation services that increases memory bandwidth and improves utilization for greater efficiency.

The Graphics Processing Cluster (GPC) is a dedicated hardware block for compute, rasterization, shading, and texturing; most of the GPU's core graphics functions are performed inside the GPC. It is comprised of Texture Processing Clusters (TPC), with each TPC containing two SM units, and a Raster Engine. The SM unit creates, manages, schedules and executes instructions from many threads in parallel. Raster operators (ROPs) continue to be aligned with L2 cache slices and memory controllers. The SM geometry and pixel processing performance make it highly suitable for rendering advanced user interfaces; the efficiency of the Volta GPU enables this performance on devices with power-limited environments.

Each SM is partitioned into four separate processing blocks (referred to as SMPs), each SMP contains its own instruction buffer, scheduler, CUDA cores and Tensor cores. Inside each SMP, CUDA cores perform pixel/vertex/geometry shading and physics/compute calculations, and each Tensor core provides a 4x4x4 matrix processing array to perform mixed-precision fused multiply-add (FMA) mathematical operations. Texture units perform texture filtering and load/store units fetch and save data to memory. Special Function Units (SFUs) handle transcendental and graphics interpolation instructions. Finally, the PolyMorph Engine handles vertex fetch, tessellation, viewport transform, attribute setup, and stream output.

Table 2 - GPU Operation

# of TPC	GPU Configuration		Performance (peak)	Max. Operating Frequency per Core
	CUDA Cores	Tensor Cores		
4	512	64	10 TFLOPS 30 TOPS	1.21GHz

¹ Feature description taken from NVIDIA® Jetson AGX Xavier™ Series System-on-Module Data Sheet.

Features:

- End-to-end lossless compression
- Tile Caching
- OpenGL 4.6, OpenGL ES 3.2, and Vulkan 1.0
- Adaptive Scalable Texture Compression (ATSC) LDR profile supported
- DirectX 12 compliant
- CUDA support
- Iterated blend, ROP OpenGL-ES blend modes
- 2D BLIT from 3D class avoids channel switch
- 2D color compression
- Constant color render SM bypass
- 2x, 4x, 8x MSAA with color and Z compression
- Non-power-of-2 and 3D textures, FP16 texture filtering
- FP16 shader support
- Geometry and Vertex attribute Instancing
- Parallel pixel processing
- Early-z reject: Fast rejection of occluded pixels acts as multiplier on pixel shader and texture performance while saving power and bandwidth
- Video protection region
- Power saving: Multiple levels of clock gating for linear scaling of power

2.4.2 Tensor Cores²

Tensor Cores and their associated data paths are custom-crafted to dramatically increase floating-point compute throughput. Each Tensor Core performs 64 floating point FMA mixed-precision operations per clock, eight Tensor Cores in an SM perform a total of 1024 floating point operations per clock. Tensor Cores operate on FP16 input data with FP32 accumulation; the FP16 multiply results in a full precision result that is accumulated in FP32 operations. Each Tensor Core provides a $4 \times 4 \times 4$ matrix processing array which performs the operation $\mathbf{D} = \mathbf{A} \times \mathbf{B} + \mathbf{C}$, where $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$ and $\mathbf{D}$ are 4×4 matrices. The matrix multiply inputs $\mathbf{A}$ and $\mathbf{B}$ are FP16 matrices, while the accumulation matrices $\mathbf{C}$ and $\mathbf{D}$ may be FP16 or FP32 matrices.

A graphical overview on this operation can be seen in Figure 1.

$$\mathbf{D} = \begin{pmatrix} \begin{matrix} A_{0,0} & A_{0,1} & A_{0,2} & A_{0,3} \\ A_{1,0} & A_{1,1} & A_{1,2} & A_{1,3} \\ A_{2,0} & A_{2,1} & A_{2,2} & A_{2,3} \\ A_{3,0} & A_{3,1} & A_{3,2} & A_{3,3} \end{matrix} & \begin{matrix} B_{0,0} & B_{0,1} & B_{0,2} & B_{0,3} \\ B_{1,0} & B_{1,1} & B_{1,2} & B_{1,3} \\ B_{2,0} & B_{2,1} & B_{2,2} & B_{2,3} \\ B_{3,0} & B_{3,1} & B_{3,2} & B_{3,3} \end{matrix} & \begin{matrix} C_{0,0} & C_{0,1} & C_{0,2} & C_{0,3} \\ C_{1,0} & C_{1,1} & C_{1,2} & C_{1,3} \\ C_{2,0} & C_{2,1} & C_{2,2} & C_{2,3} \\ C_{3,0} & C_{3,1} & C_{3,2} & C_{3,3} \end{matrix} \end{pmatrix}$$

FP16 or FP32
FP16
FP16
FP16 or FP32

Source: Nvidia®

Figure 1 - Matrix processing

² Tensor Cores description is taken from NVIDIA® Xavier™ Series System-on-Chip Technical Reference Manual

2.4.3 Carmel CPU Complex

The CPU complex (CCPLEX) is comprised of Carmel dual-core CPU clusters in a coherent multi-processor configuration. A high-performance System Coherency Fabric (SCF) connects all CPU clusters enabling simultaneous operation of all CPU cores (as needed) for a true heterogeneous multi-processing (HMP) environment. The SCF also connects CPU clusters to:

- DRAM through the Memory Controller Fabric (MCF).
- Other processing and I/O blocks in the Memory Mapped I/O (MMIO) space through an ARM Advanced eXtensible Interface (AXI).

Each CPU cluster contains two identical Carmel processors; each core includes 128 KB Instruction (I-cache) and 64 KB Data (D-cache) Level 1 caches, a 2 MB L2 cache is shared by both cores.

Table 3 - CPU Operation

CPU Configuration			CPU Cores	Max. Operating Frequency per Core*
CPU Cluster	L2 Cache	L3 Cache		
4x dual core	8MB	4MB	8	2.03GHz

* Refer to the documentation provided with each software release for additional information on supported power modes and CPU operation.

Features:

- NVIDIA® Dynamic Code Optimization
- 10-wide Superscalar architecture
- Dynamic branch prediction with a Branch Target Buffer and Global History Buffer RAMs, a return stack buffer, and an indirect predictor.
- Full implementation of ARMv8.2 ISA compliant architecture including:
 - o ARMv8 TrustZone
 - o ARMv8.0 Crypto ISA
 - o Trusted Memory
 - TZ-RAM
 - TZ-DRAM
 - Dynamic CMA VPR
 - GSC DRAM Carveouts
 - Clock Monitoring
 - Voltage Monitoring
 - Trusted Boot
 - Trusted Debug
 - o ARMv8.2-FP16 support
- 128 KB 4-way-associative parity protected L1 instruction cache per core
- 64 KB 4-way-associative parity protected L1 data cache per core
- 2 MB 16-way-associative ECC protected L2 cache per CPU cluster
- 4 MB 16-way-associative ECC protected L3 cache (shared across all clusters)
- Performance Monitoring
- Interface to an external Generic Interrupt Controller (vGIC-400)
- Support for power management with multiple power domains

2.4.4 Memory Subsystem

The Memory Subsystem (MSS) provides access to local DRAM, SysRAM, and provides a SyncPoint Interface for inter-processor signaling. The memory subsystem supports full-speed I/O coherence by routing requests through a scalable coherence fabric. It also supports a comprehensive set of safety and security mechanisms.

Structurally, the MSS consists of:

1. MSS Data Backbone - routes requests from clients to the MSS Hub and responses from MSS Hub to the clients.
2. MSS Hub - receives and arbitrates among client requests, performs SMMU translation, and sends requests to the MCF.
3. Memory Controller Fabric (MCF) - performs security checks, feeds I/O coherent requests to the Scalable Coherence Fabric (SCF), and directs requests to the multiple memory channels.
4. Memory Controller (MC) Channels - row sorter/arbitrator and DRAM controllers.
5. DRAM IO - channel-to-pad fabric, DRAM I/O pads, and PLLs.

Xavier™ series modules integrate a 256-bit wide LPDDR4X memory interface implemented as eight 32-bit channels with x16 subpartitions. The memory controller provides a single read or write command and row address to both sub-partitions in the channel to transfer 64 bytes, but provides three independent column address bits to each sub-partition, allowing it access different 32 byte sectors of a GOB between the sub-partitions. It provides connections between a wide variety of clients, supporting their bandwidth, latency, quality-of-service needs and any special ordering requirements that are needed. The MSS supports a variety of security and safety features and address translation for clients that use virtual addresses.

Table 4 - LPDDR4x Memory Bus

Size	Maximum Bandwidth	Maximum Bus Frequency	ECC Support
32GB	136.5GB/s	2133MHz	Enabled by software

Features:

- LPDDR4X: x32 DRAM chips
- 256-bit wide data bus
- Low Latency Path and Fast Read/Response Path Support for the CPU Complex Cluster
- Support for low-power modes:
 - o Software controllable entry/exit from: self-refresh, power down, deep power down
 - o Hardware dynamic entry/exit from: power down, self-refresh
 - o Pads use DPD-mode during idle periods
- High-bandwidth interface to the integrated Volta GPU
- Full-speed IO coherence with bypass for Isochronous (ISO) traffic
- System Memory-Management Unit (SMMU) for address translation based on the ARM SMMU-500
- High-bandwidth PCIe ordered writes
- AES-XTS encryption with 128-bit key
- DRAM ECC (enabled by software)
 - o SEC (Single Error Correction)
 - o DED (Double Error Detection)
 - o Parity protection support

2.5 Board Diagrams

The following diagrams provide an overview on the JetKit-3010 components and interfaces.

2.5.1 Block Diagram

Figure 2 and Figure 3 show the simplified block diagrams of the Elma JetKit-3010 baseboard and the mezzanine board.

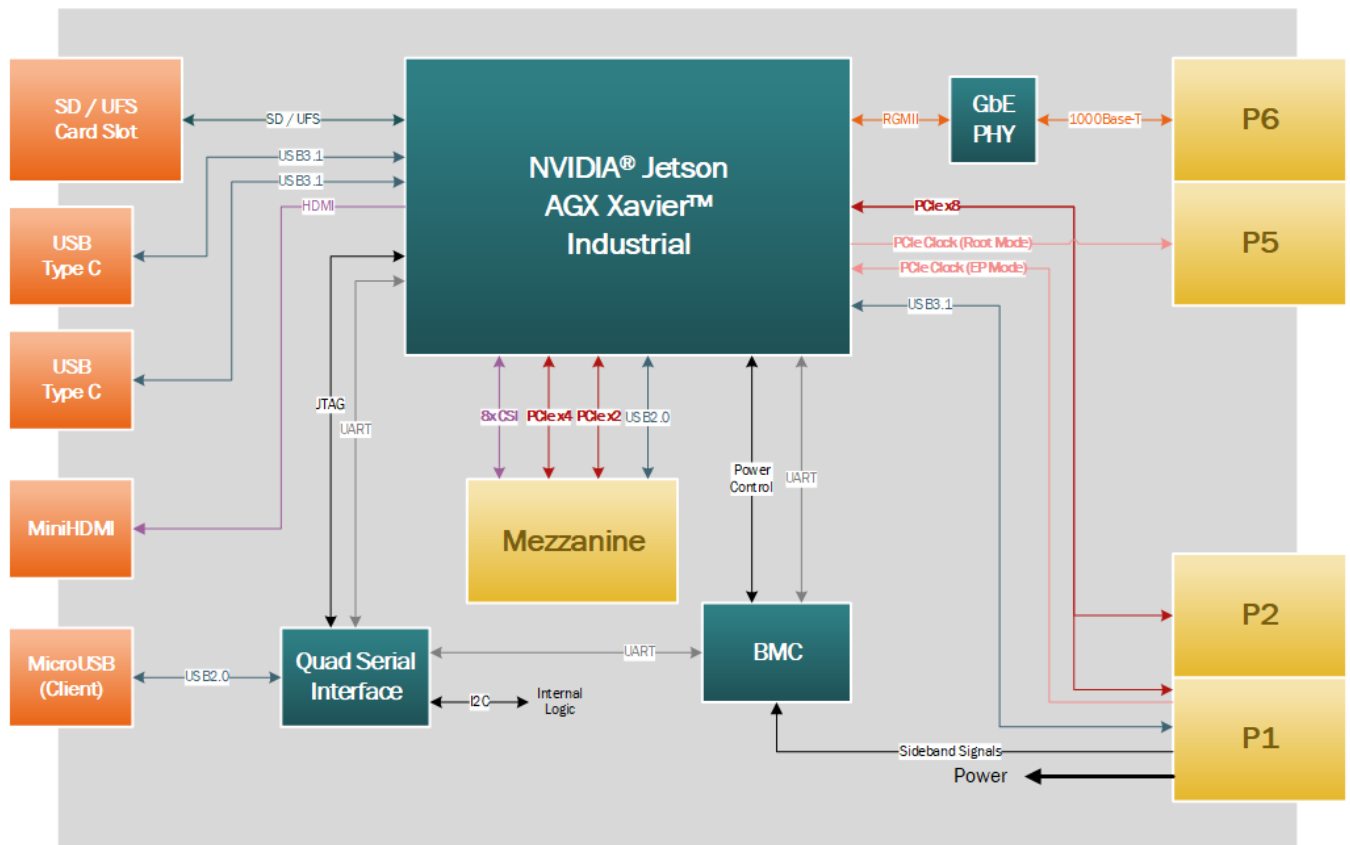


Figure 2 - Simplified Block Diagram

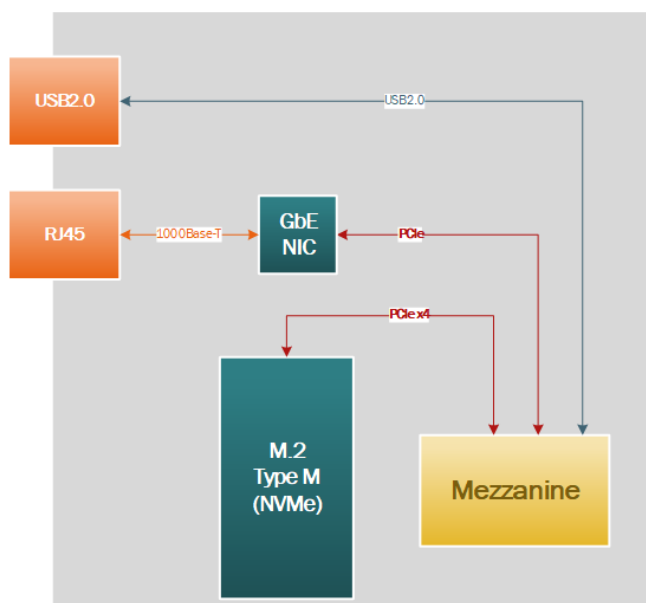


Figure 3 - Mezzanine Block Diagram

2.5.2 Front Panel

Figure 4 shows the front panel of the JetKit-3010.

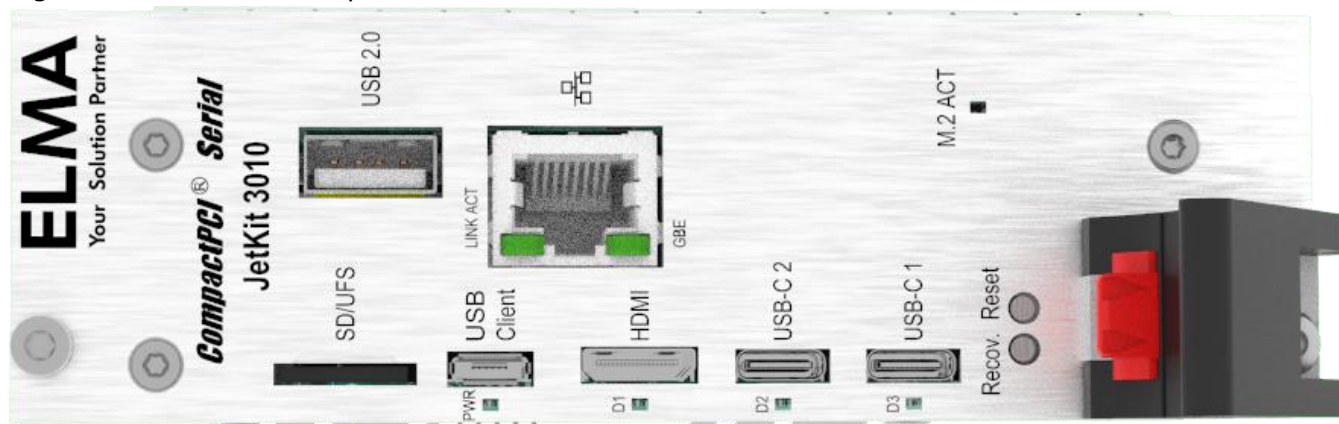


Figure 4 - Front Panel

PWR: Power LED – lit as soon as Power is provided for the NVIDIA® Xavier™ module.

D1/D2/D3: User LEDs are controlled by GPIOs from the NVIDIA® Xavier™.

D1/2: green
D3: red

SD/UFS: MicroSD / UFS card socket

USB Client: USB client port to provide access to BMC and NVIDIA® Xavier™ console ports.

HDMI: MicroHDMI connector with HDMI 2.0a/b compliant interface

USB-C 1/2: USB Type C connectors with USB3.1/2.0 interfaces
USB-C 1 provides Device functionality for programming.

Recov.: NVIDIA® Xavier™ Recovery Button.

Note: For Recovery functionality, the button must be pressed during power up or reset of the NVIDIA® Xavier™. Power up of the NVIDIA® Xavier™ takes ~3 seconds after powering / reset of the board for BMC booting.
The Power LED provides indication when the NVIDIA® Xavier™ is powered.

Reset: Reset Button for Board reset

USB2.0: USB2.0 interface of the NVIDIA® Xavier™

: 1000Base-T RJ45 Ethernet interface.
LINK/ACT: Link / Activity LED
GBE: 1000Mbit/s Link

M.2 ACT: Activity of M.2 module

2.5.3 Board assembly

The images in the following show the complete board with NVIDIA® module, heat sinks and mezzanine (Figure 5) and with NVIDIA® module, but without heat sinks and mezzanine (Figure 6).

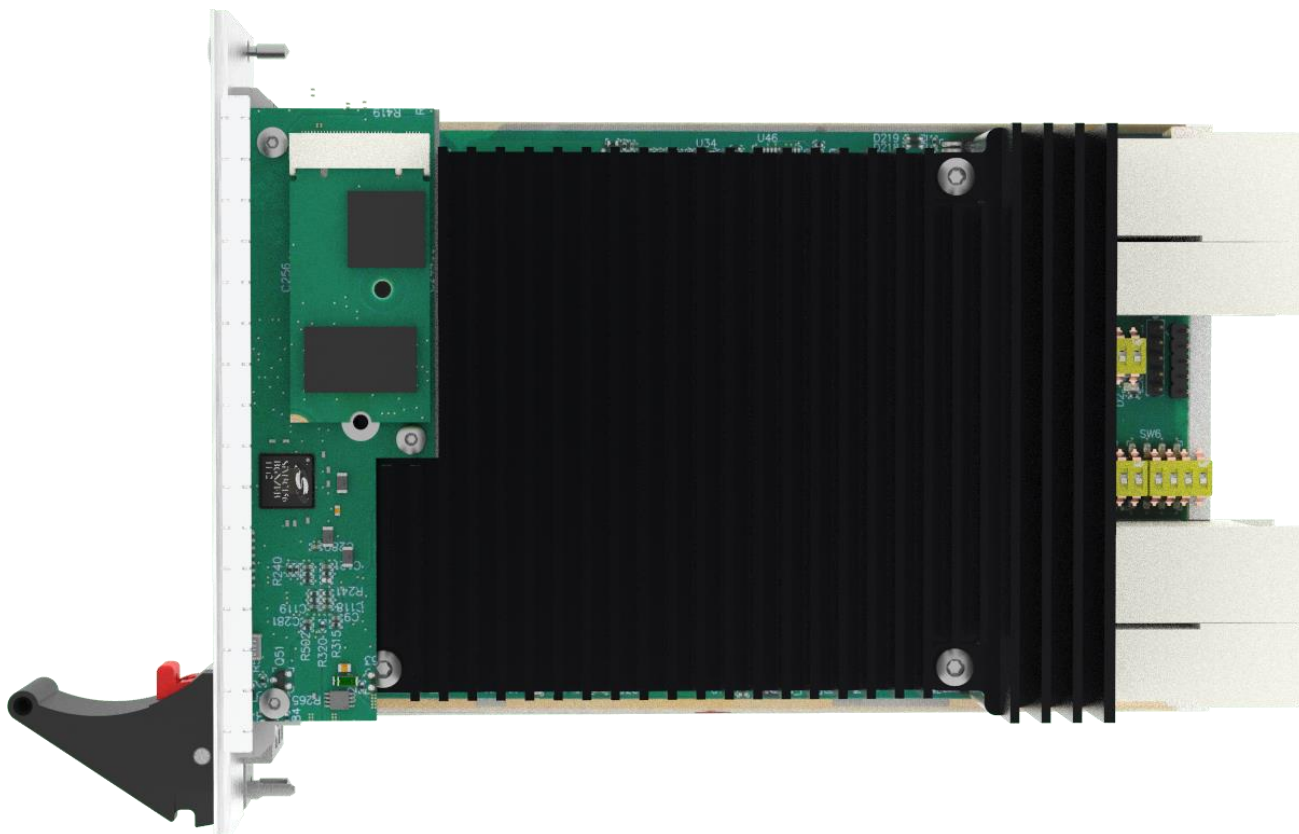


Figure 5 - Board with NVIDIA® module, heat sinks and mezzanine

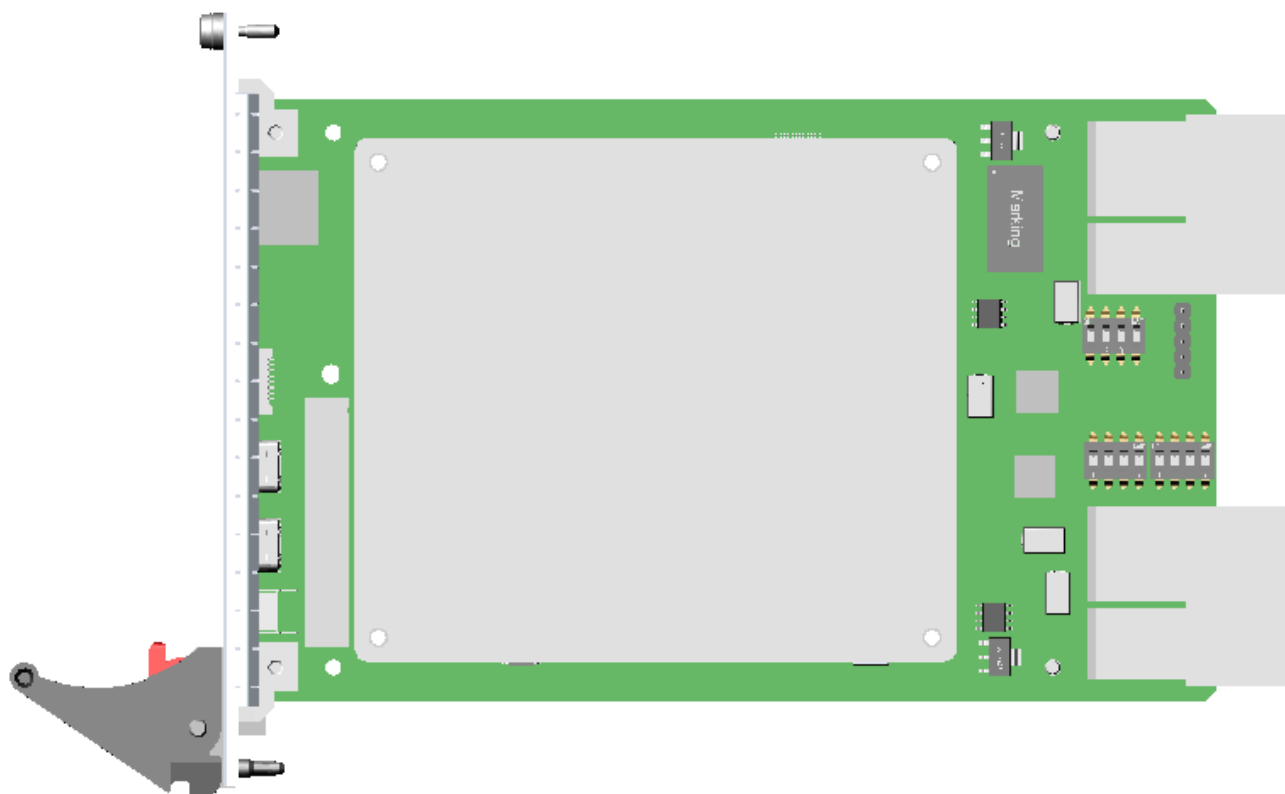


Figure 6 - Board with NVIDIA® module, without heat sinks and mezzanine

2.5.4 Baseboard layout

In the following, Figure 7 and Figure 8 show the baseboard top and bottom view, highlighting the positons of the main components. Table 5 lists the components by number.

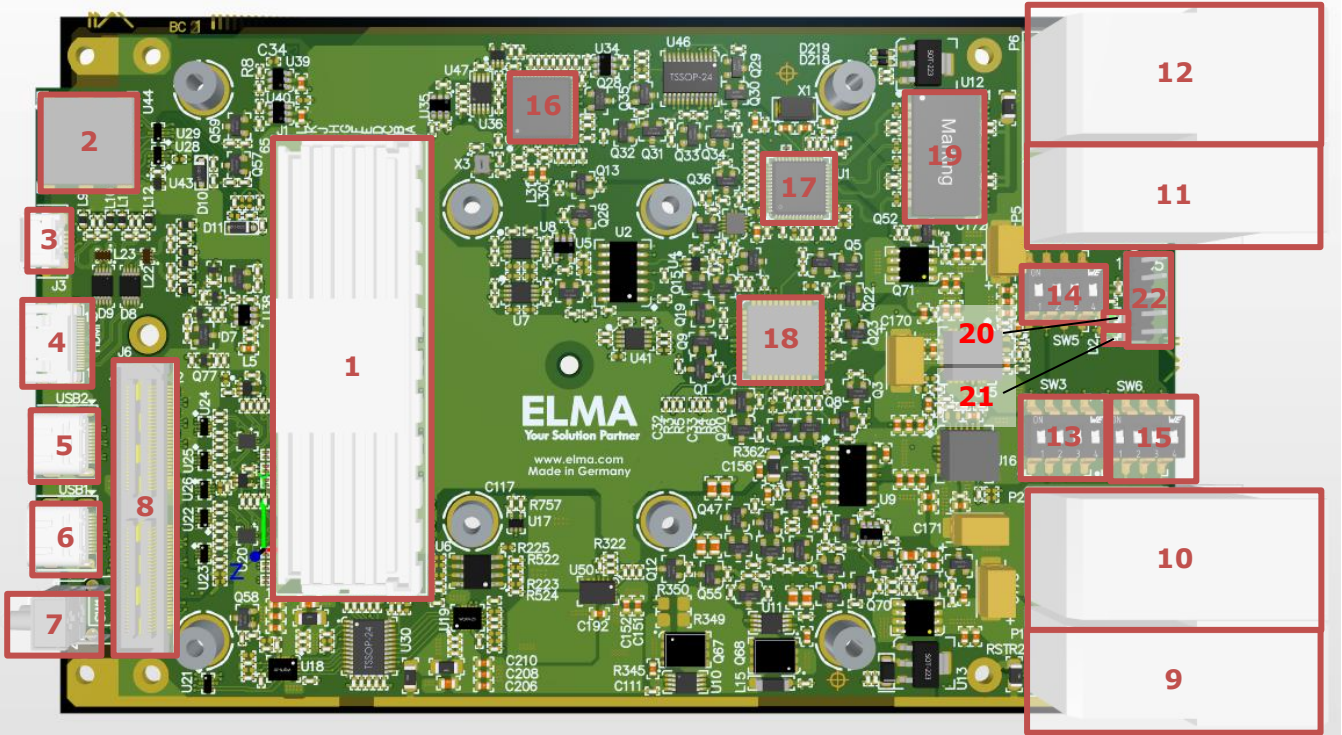


Figure 7 - Baseboard top components

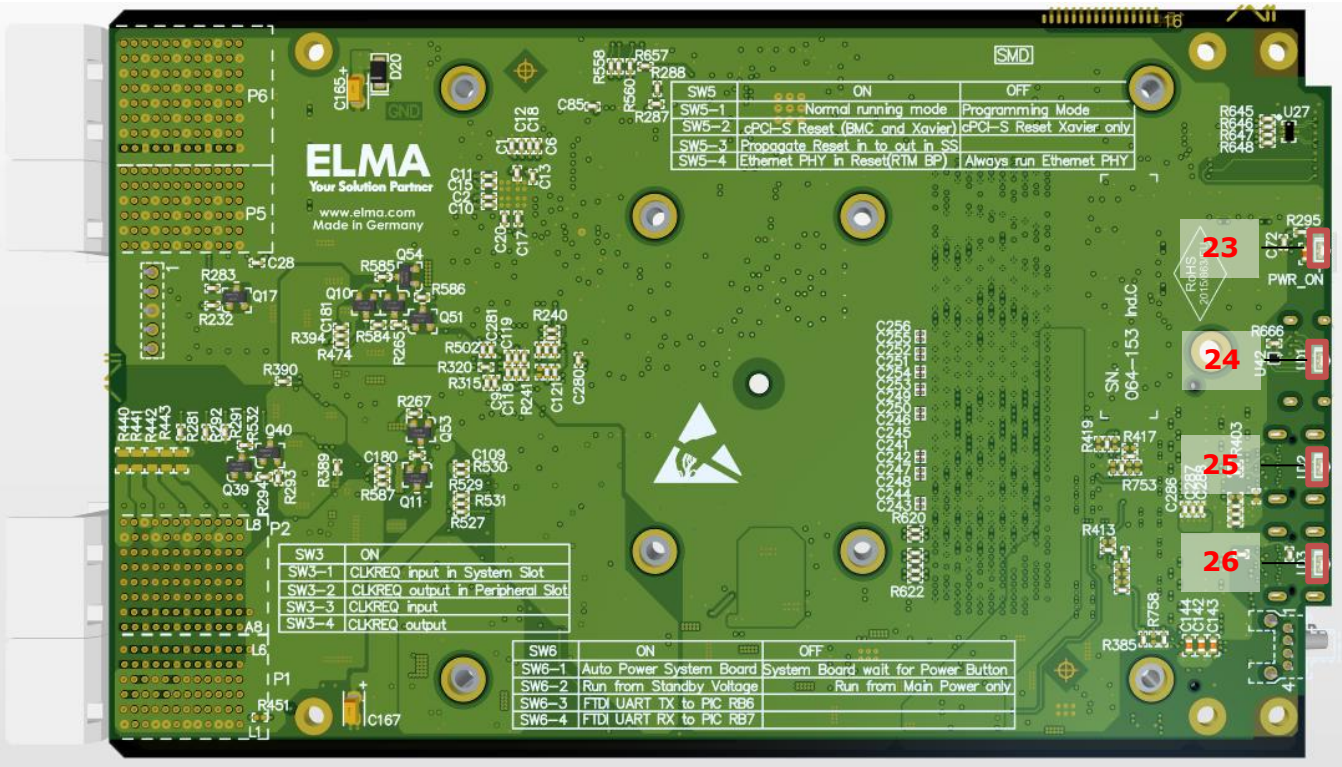


Figure 8 - Board bottom components

Table 5 – Board main components

#	Side	RefDes	Description
1	Top	J1	NVIDIA® Xavier™ module connector
2	Top	U44	MicroSD/UFS card socket
3	Top	J3	MicroUSB client connector
4	Top	HDMI	MiniHDMI connector
5	Top	USB2	USB type C connector (USB-C 2 interface)
6	Top	USB1	USB type C connector (USB-C 1 interface)
7	Top	SW1	Reset and Recovery Button
8	Top	J6	High-speed mezzanine connector
9	Top	P1	CompactPCI Serial P1 connector
10	Top	P2	CompactPCI Serial P2 connector
11	Top	P5	CompactPCI Serial P5 connector
12	Top	P6	CompactPCI Serial P6 connector
13	Top	SW3	DIP switch SW3
14	Top	SW5	DIP switch SW5
15	Top	SW6	DIP switch SW6
16	Top	U36	USB quad UART
17	Top	U1	Ethernet PHY
18	Top	U3	BMC
19	Top	T1	Ethernet Magnetics
20	Top	D1	PHY LED0 (Link)
21	Top	D2	PHY LED1 (ACT)
22	Top	J5	BMC Prog programming header
23	Bottom	PWR_ON	Power On LED (green)
24	Bottom	LD1	User LED 1 (green)
25	Bottom	LD2	User LED 2 (green)
26	Bottom	LD3	User LED 3 (red)

2.5.5 Mezzanine Layout

In the following, Figure 9 and Figure 10 show the baseboard top and bottom view, highlighting the positions of the main components. Table 6 lists the components by number.

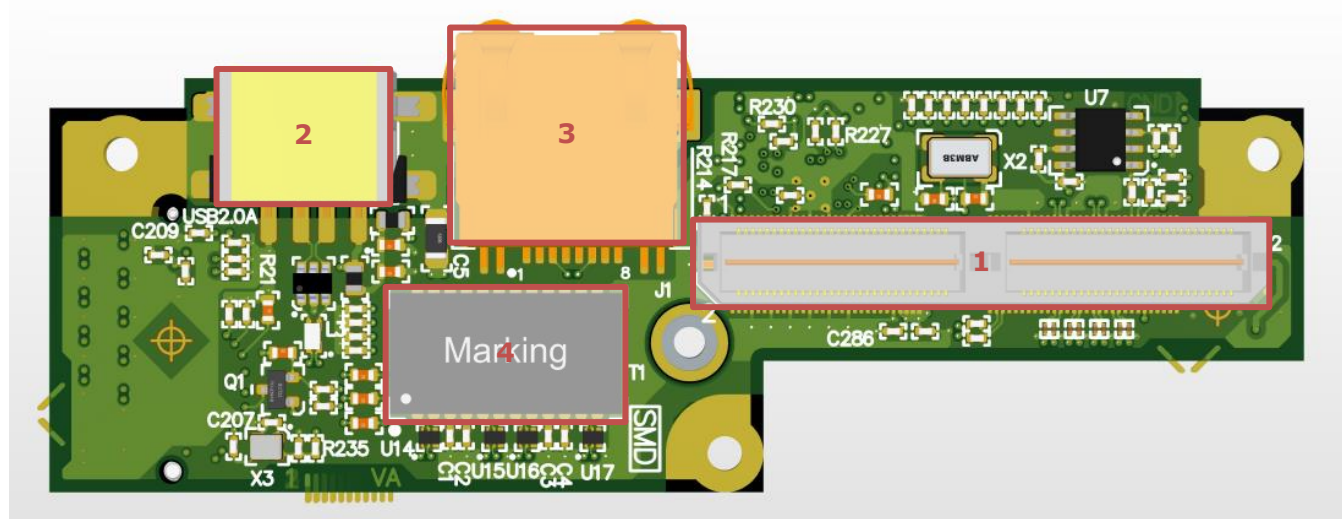


Figure 9 - Mezzanine top components

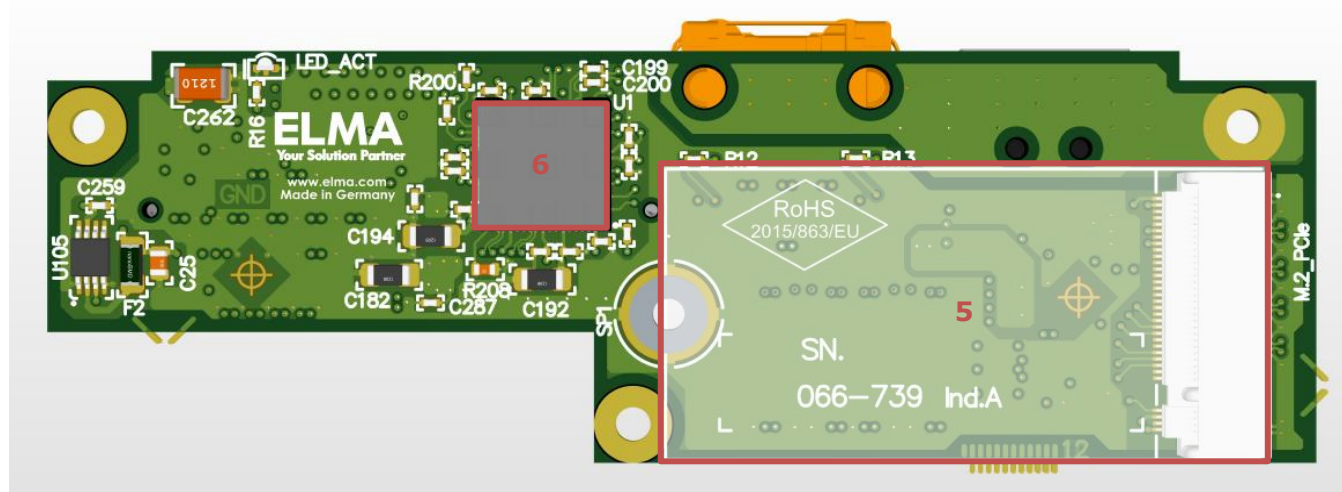


Figure 10 - Mezzanine bottom components

Table 6 – Mezzanine main components

#	Side	RefDes	Description
1	Top	J6	High-speed mezzanine connector
2	Top	USB2.0A	USB2.0 connector
3	Top	J1	RJ45 connector
4	Top	T1	Ethernet magnetics
5	Bottom	M.2_PCIe	M.2 socket
6	Bottom	U1	Ethernet NIC (Intel i210-AT)

3 Functional Description

3.1 CompactPCI Serial operation

The JetKit-3010 can be operated in a CompactPCI Serial compliant system slot or peripheral slot. Used in a system slot, the board can control and receive the sideband signals available on the system slot to control the power management of the rack and the boards. Used in a peripheral slot, the sideband signals are ignored. In both cases, the I²C System Management Bus is ignored, but can be implemented on a custom base.

The different usages of the sideband signals are listed in Table 7.

Table 7 - CompactPCI Serial Sideband Signals

Connector	Pin	System Slot Functionality	Peripheral Slot Functionality
P1	E2	PS_ON#	Ignored
P1	F2	Reset Output	Ignored
P1	H2	Pushbutton Reset (Reset Input)	Reset Input
P1	I2	WAKE_IN#	WAKE_OUT# - Unused
P1	K2	PCIE_EN# - See chapter 3.2	PCIE_EN# - See chapter 3.2
P1	L2	SYSEN# (GND on system slot)	SYSEN# (open on peripheral slot)
P1	C3	PWRBTN#	GA0
P1	F3	PWR_FAIL#	GA1
P1	I3	GA2 (GND)	GA2
P1	L3	GA3 (GND)	GA3
P1	E4/F4	PE_CLKIN+/- - See chapter 3.2	PE_CLKIN+/- - See chapter 3.2
P5	A5/B5	1_PE_CLK+/- - See chapter 3.2	1_PE_CLK+/- - See chapter 3.2
P5	C5	1_PE_CLKE# - See chapter 3.2	1_PE_CLKE# - See chapter 3.2

The board automatically detects the slot type by reading the SYSEN# pin and changes the role accordingly.

The power control options when acting as system board can be configured by using DIP switches on the board. See chapter 3.5 for more information about the power control options. See Table 34 in chapter 4 for information about the power-related DIP switch settings.

3.2 PCI Express operation

3.2.1 Overview

The PCI Express functionality in CompactPCI Serial is specified in that way that the system board is the PCI Express complex and the peripheral boards are PCI Express end points.

The JetKit-3010 does not control the PCI Express role according to the slot type plugged. Instead, the PCI Express root or end point functionality are configured via software of the NVIDIA[®] Xavier™. This allows special configurations e.g. where the JetKit-3010 can be plugged in a peripheral slot, but still works in PCI Express root mode, e.g. in conjunction with a (non-transparent) PCI Express switch.

By default, the NVIDIA[®] Xavier™ works in root mode. To configure the NVIDIA[®] Xavier™ for an end point, consult the NVIDIA[®] documentation at:

<https://docs.nvidia.com/jetson/archives/r34.1/DeveloperGuide/text/SD/Communications/JetsonAgxXavierPcieEndpointMode.html>

3.2.2 [PCI Express clock](#)

The NVIDIA® Xavier™ has two distinct PCI Express clocks for the PCI Express interfaces. There is one PCI Express clock used as input and a separate PCI Express clock used as output.

The clock output signals PEX_CLK5_P/N of the NVIDIA® Xavier™ are connected to the CompactPCI Serial clock outputs 1_PE_CLK+/- in connector P5, pins A5/B5 (system slot pinout).

The clock input signals NVHS0_REFCLK_P/N are connected to the CompactPCI Serial clock input PE_CLKIN+/- in connector P1, pins E4/F4 (peripheral slot pinout).

In contrast to those distinct clock signals, there is just a single CLKREQ# signal on the NVIDIA® Xavier™ (PEX_L5_CLKREQ_N). Depending on the direction of the clock signals used, the CLKREQ# signal is used in the opposite direction to either request an incoming clock or detect a request for an outgoing clock.

Both those CLKREQ# functionalities use different pins in the CompactPCI Serial slot. The CLKREQ# input (1_PE_CLKE# for PCI Express clock signals 1_PE_CLK+/-) is located on connector P5 pin C5 (system slot pinout). The CLKREQ# output (PCIE_EN#) is located on connector P1, pin K2 (peripheral slot pinout).

On the peripheral slot pinout, connector P5 pin C5 is a GND pin. So the CLKREQ# input and output pins should not be interconnected. Therefore, the desired direction can be configured on the board. See Table 32 in chapter 4 for the DIP switch settings to select the CLKREQ# input/output pin configuration.

3.2.3 [PCI Express reset](#)

The PCI Express link of the JetKit-3010 has a dedicated reset signal (PEX_L5_RST_N). Depending on the operation mode of the PCI Express link, the direction of the signal is inverted. In PCI Express root mode, the reset signal is an output to trigger the reset of the PCI Express nodes.

When in endpoint mode, the reset signal is an input to be triggered by the root complex.

The CompactPCI Serial architecture does not provide a separate PCI Express reset on the connector pinout. Therefore, the reset signal is connected to the BMC, which allows propagation of the PCI Express reset to the main reset output on the backplane, when the PCI Express reset is an output of the NVIDIA® Xavier™. When the PCI Express reset is an input (endpoint mode), the reset input of the board can be used to trigger the PCI Express reset of the NVIDIA® Xavier™.

This PCI Express reset configuration can be configured via "config" command in the BMC CLI (see chapter 3.3.2).

3.3 Board Management Controller (BMC)

3.3.1 [Overview](#)

The BMC of the JetKit-3010 acts as the power management controller for the NVIDIA® AGX Xavier™ module. This module requires a certain power up sequence to run the module reliably, which is implemented by the BMC. The BMC further needs to consider the CompactPCI Serial role (system / peripheral board) as well as power control options.

Additionally, the BMC acts as voltage monitor and reset controller, which handles the reset input and output signals from the CompactPCI Serial backplane, the main reset as well as the PCI Express reset of the NVIDIA® Xavier™.

3.3.2 Command Line Interface (CLI)

The BMC's CLI can be accessed via the front MicroUSB connector. This interface provides access to four ports, where the two last ones are used serial ports. See Table 15 for the list of interfaces provide by the MicroUSB interface. The third interface available provides access to the CLI of the BMC. The serial port settings for this interface can be found in Table 8.

Table 8 - BMC CLI serial port settings

Parameter	Setting
Baud rate	115200
Data bits	8
Parity	None
Stop bits	1

The CLI supports "arrow up" and "arrow down" to parse between the last commands to be able to repeat those commands without retyping. Up to 10 commands are stored. In addition, manipulation of the stored commands after recalling is possible (helps to correct typing errors). The CLI allows access to status information and manipulation. The following commands are available in the CLI:

help / ?:

Displays the available commands.

config:

Displays or modifies the configuration of the board.

Configuration settings are to manage Off/Reset control, Reset handling etc.

info:

Shows board information like slot type and number, power control configuration and power state.

ios:

Provides information about the status of the BMC I/Os and allows manipulation of outputs.



Use manipulation of the outputs with care!
Manipulate outputs only, if you know what you are doing!

To manipulate outputs, type:

`ios output_name output_level`

`output_name:` signal name (e.g. "VIN_PWR_ON") or output number (e.g. "RD0")

`output_level:` "0" or "low" to set the output low
"1" or "high" to set the output high



Outputs, which are modified by automatic BMC functionality (e.g. reset or power control), overwrite the manual output settings.

reset:

This command resets the BMC, which also resets the NVIDIA® Xavier™.

version:

Display BMC Firmware version.

volt / voltage:

Display the board voltages. The voltages, which are displayed, are listed in Table 9.

Table 9 - Measured board voltages

Displayed Voltage	Description
12V	12V received from the CompactPCI Serial Backplane
SYS_VIN_HV	12V connected to the NVIDIA® Xavier™
5V STDBY	5V Standby received from the CompactPCI Serial Backplane
3V3	3.3V generated by an on-board DC/DC converter
1V8	1.8V generated by an on-board DC/DC converter
5V	5V generated by an on-board DC/DC converter
SYS_VIN_MV	5V connected to the NVIDIA® Xavier™

SYS_VIN_HV and SYS_VIN_MV are the 12V respective 5V supply voltages of the NVIDIA® Xavier™ module. Both are not allowed to be active at all times when the respective supply voltages are available. Therefore, those voltages are switched on separately via MOSFETs from the BMC.

redirect:

Due to the additional CLI of the BMC, there is one less available port on the MicroUSB interface connector, compared to the NVIDIA® Xavier™ Developer Kit.

To enable the usage of this additional serial interface of the NVIDIA® Xavier™, this port has been connected to a second serial port of the BMC. The command redirects any inputs and outputs between the NVIDIA® Xavier™ and the BMC interface.

STRG + C ends redirection.

3.3.3 *Firmware Update*

The BMC includes a UART bootloader, which allows the board being updated via the MicroUSB port. To update the Firmware of the BMC, the "Microchip Unified Bootloader Host Application" is required. The application can be downloaded from the Microchip website:

<https://www.microchip.com/promo/8-bit-bootloader>

Scroll down and switch to the "Software" tab or use the direct download link (current version V1.18.0 of the time of release of this documentation):

<https://www.microchip.com/mymicrochip/filehandler.aspx?ddocname=en1000558>

To update the BMC, connect to the BMC CLI. For details about how to connect to the CLI, see chapter 3.3.2.

Start the board or – if already running – type the command "reset" to reset the board. Stop the board from running the main application by pressing "x" within 2 seconds after (re-)start.

Disconnect the terminal program from the serial port to make the port available for the update tool. Start the "Microchip Unified Bootloader Host Application".

The main window of the bootloader application is shown in Figure 11.

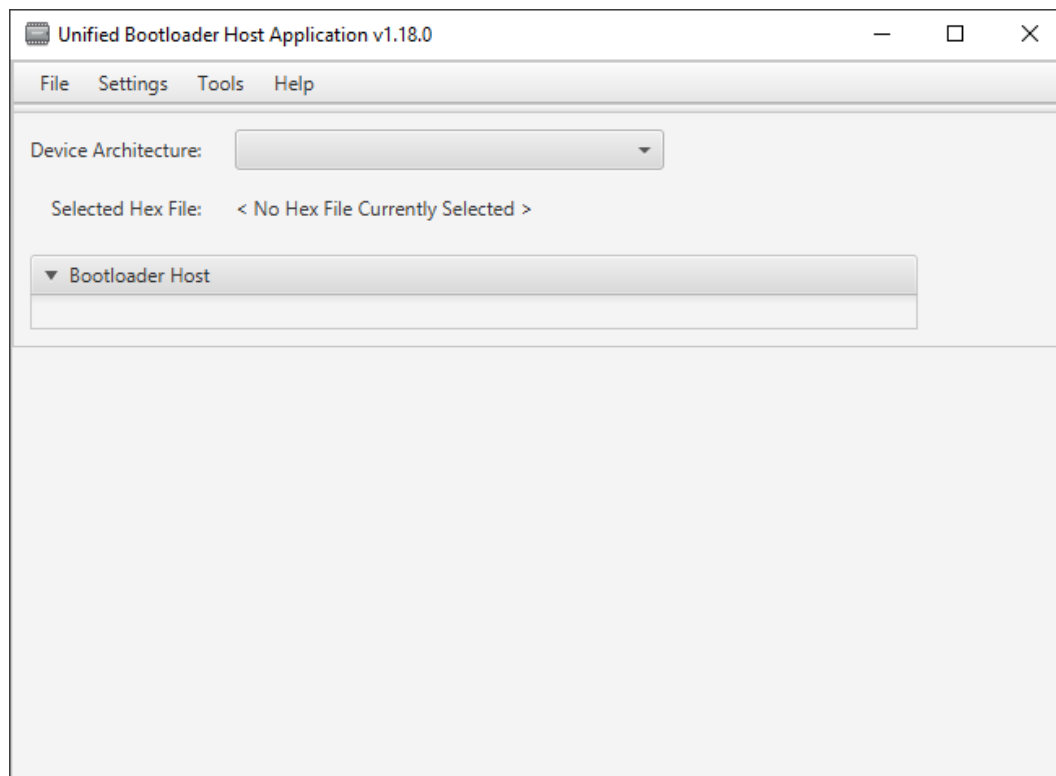


Figure 11 - Bootloader Main Window

Select the Firmware .hex file from the File -> Open/Load File (*.hex) menu. The selected file is show in the main window (see Figure 12).

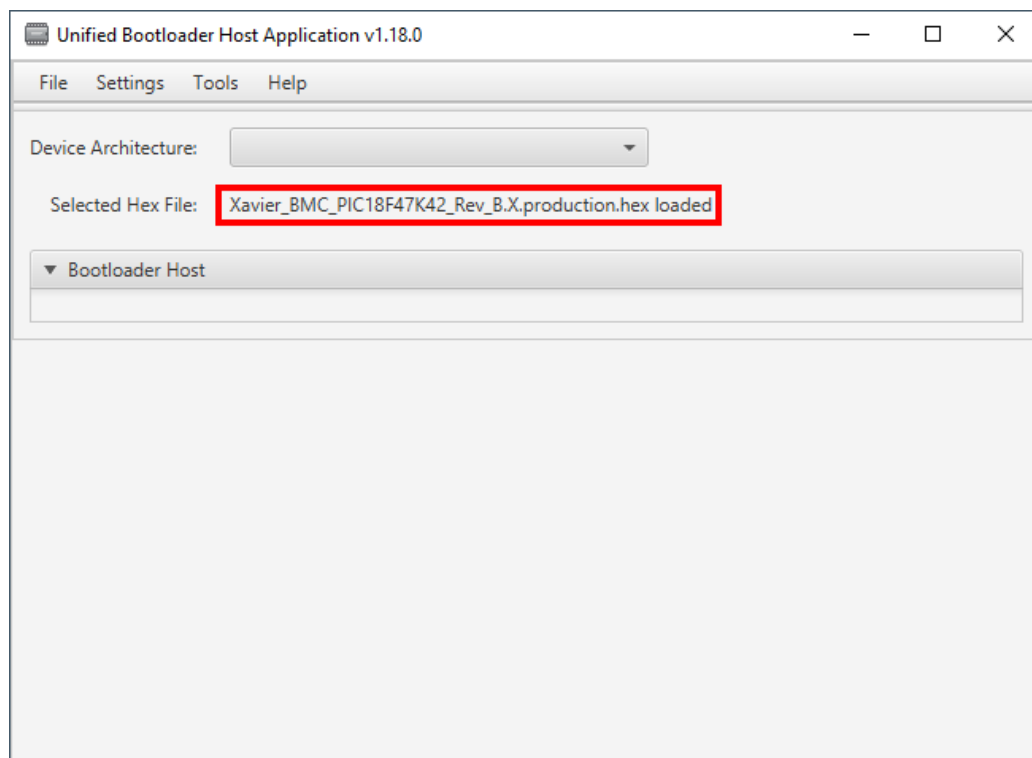


Figure 12 - Bootloader application with selected Firmware File

Select the device architecture "PIC10\PIC12\PIC16\PIC18 MCUs" and the 8-Bit Architecture "PIC18" as shown in Figure 13.

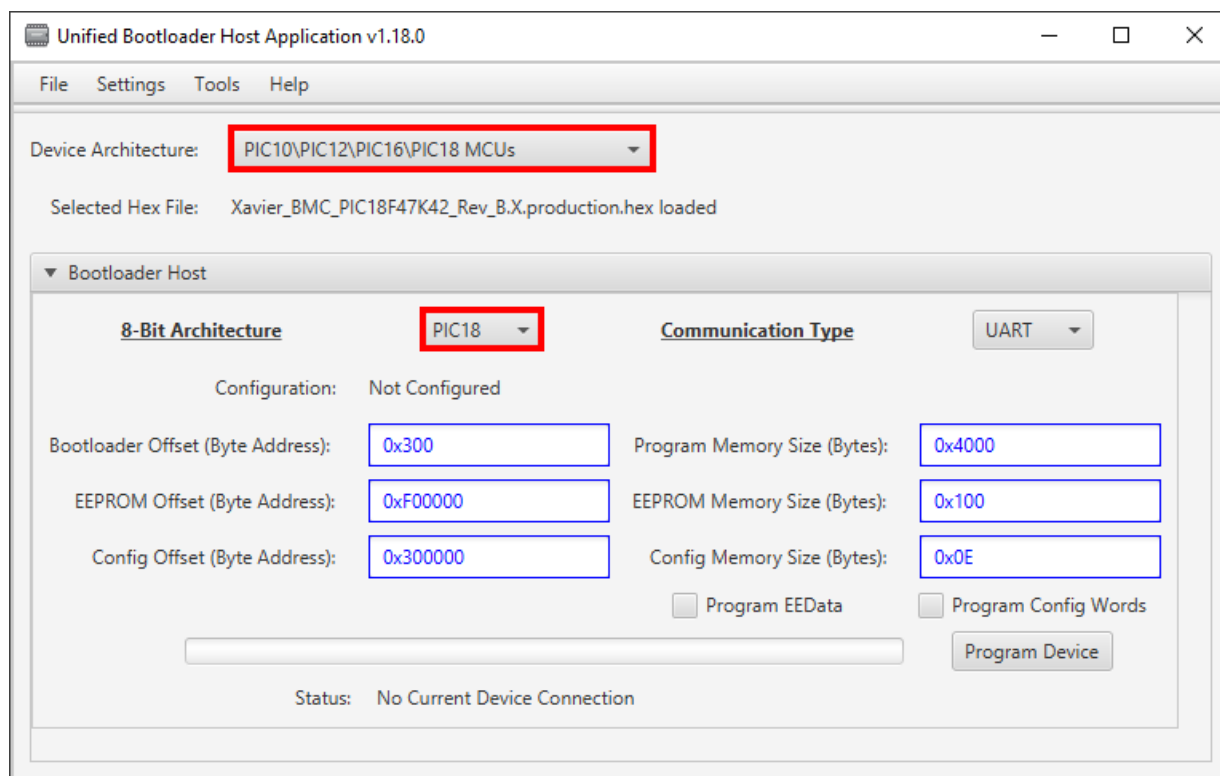


Figure 13 - Bootloader application with selected MCU architecture

Open the serial port configuration window from the Settings -> Serial menu. Select the COM port to the BMC and configure the serial port settings as shown in Figure 14.

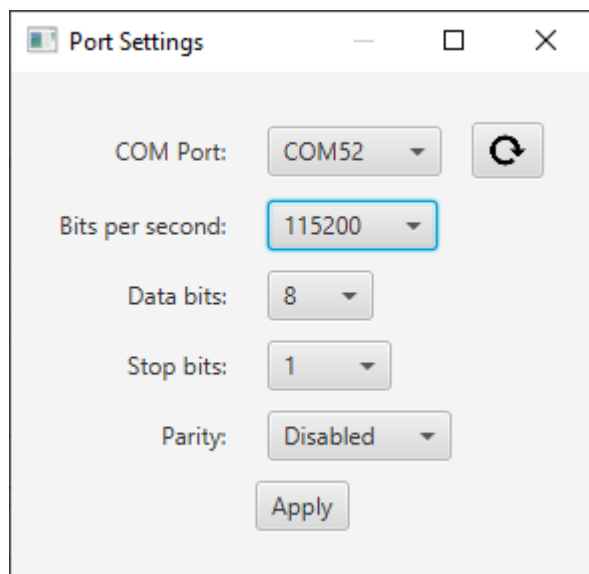


Figure 14 - Bootloader serial port settings

Modify the Byte (Address) settings and enable “Program Config Words” according to Figure 15.

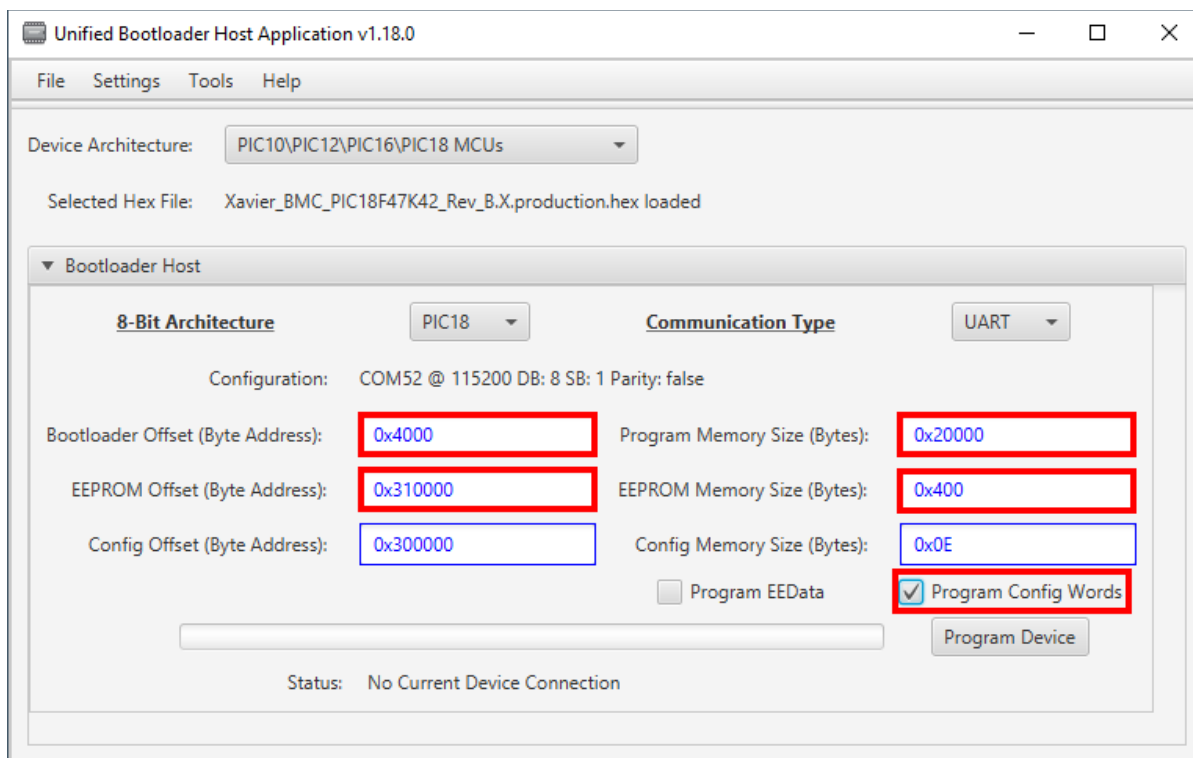


Figure 15 - Bootloader application configured for BMC update

After this configuration, press “Program Device” to start the update. When the update is finished, the new Firmware is automatically started.

3.4 USB Type C interface management

The Xavier™ board provides two USB type C interface connectors.

To avoid feeding the board from an external USB type C charger / host device, the power delivery controller used on the Developer Kit has been replaced by a simpler one, which prevents feeding the Xavier™ board from USB.



The default firmware of the NVIDIA® Xavier™ used for the Developer Kit tries to access the original PD controller. If this cannot be found, the Xavier™ cannot gather the USB mode (host / OTG). Therefore, the Device Tree needs to be modified and the OTG mode needs to be removed to be able to use the USB interfaces.

The selected USB PD controller does not require any software implementation, but works autonomously. The PD controller detects the cable polarity and UFP/DFP configuration of the attached device. According to the detected configuration, the PD controller manages the power output and USB3 compliant multiplexer used to support cable flip.

In the default configuration, the PD controller advertises support for 1.5 A @5V power supply capability. The PD controller current advertisement can be found in Table 11.

It is possible to read and modify some parameters of the PD controller using an I²C IO expander, which connects to some configuration inputs and status indicator outputs of the PD controller. The I²C IO expander is located on I²C bus 1 with chip address 0x74. The IO status can e.g. be gathered with the Linux command `i2cget -y 1 0x74 0 w`

Please note that word reading swaps the two bytes of the answer.

The IO signal meaning of the IO expander can be found in Table 10.

Table 10 - IO Expander IOs for PD controller configuration / indication

Port	USB Port	Signal	I / O*	Default	Description
P00	USB-C 1	EN	O	High	Enable signal for PD controller high – enabled low – disabled
P01	USB-C 1	CHG	O	High	Charger configuration inputs. CHG in conjunction with CHG_HI control the power delivery capability. Configuration settings see Table 11.
P02	USB-C 1	CHG_HI	O	Low	
P03	USB-C 1	FAULT#	I	-	Fault indicator output low – current-limiting or thermal shutdown
P04	USB-C 1	LD_DET#	I	-	High charging current detected. Load threshold see Table 11.
P05	USB-C 1	UFP#	I	-	Upstream Facing Port detect high – Downstream Facing Port / no connection low – Upstream Facing Port connected This signal can be used to switch host / OTG mode.
P06	USB-C 1	POL#	I	-	Polarity detect high – Standard polarity / no cable connected low – Flipped cable connected This signal is used to control the multiplexer for the super speed lines.
P07	USB-C 1	AUDIO#	I	-	Audio accessory detect** low – audio accessory detected
P10	USB-C 2	EN	O	High	Enable signal for PD controller high – enabled low – disabled
P11	USB-C 2	CHG	O	High	Charger configuration inputs. CHG in conjunction with CHG_HI control the power delivery capability. Configuration settings see Table 11.
P12	USB-C 2	CHG_HI	O	Low	
P13	USB-C 2	FAULT#	I	-	Fault indicator output low – current-limiting or thermal shutdown
P14	USB-C 2	LD_DET#	I	-	High charging current detected. Load threshold see Table 11.
P15	USB-C 2	UFP#	I	-	Upstream Facing Port detect high – Downstream Facing Port / no connection low – Upstream Facing Port connected This signal can be used to switch host / OTG mode.
P16	USB-C 2	POL#	I	-	Polarity detect high – Standard polarity / no cable connected low – Flipped cable connected This signal is used to control the multiplexer for the super speed lines.
P17	USB-C 2	AUDIO#	I	-	Audio accessory detect** low – audio accessory detected

*Input / Output is seen from IO Expander. PD controller direction is opposite.

**The JetKit-3010 does not support audio accessories.

Table 11 - PD controller current advertisement

CHG	CHG_HI	CC Capability Broadcast	Current Limit (typical)	Load Detect threshold (typ.)
0	0	STD	1.7 A	N/A
0	1	STD	1.7 A	N/A
1	0	1.5 A	1.7 A	N/A
1	1	3 A	3.4 A	1.95 A



The maximum 5V current capability of the JetKit-3010 is 8 A. This current is shared between the BMC including additional logic components, the NVIDIA® Xavier™ (SYS_VIN_MV) and the USB ports.

Modifications of the charging current is under own risk and can make the board unstable in case of an overcurrent!

3.5 Power Management

The BMC of the JetKit-3010 is ready to support an ATX based or AT based system.

AT based systems are designed supporting only main voltages. In case of a CompactPCI Serial based system, this means that only 12V is available.

An ATX based system provides also a standby voltage, i.e. 5V standby in CompactPCI Serial.

To support both, the BMC can be operated from 5V standby directly or from 5V generated by the 12V main voltage. In case operation from 5V standby is not desired, the board provides the option to disable 5V standby support.

In ATX mode, a system normally provides 5V standby as soon as primary power is applied. To enable main power, the PSU needs to be enabled. In a CompactPCI Serial based system, the signal PS_ON# needs to be pulled to GND to enable the PSU main power.

The BMC can be configured for two operations:

- Auto Power: Enables the PS_ON# as soon as the BMC has booted up
- Manual Power: Waits for a power on event. Power on events are:
 - o Power Button press (via PWRBTN# signal)
 - o Wake event (via WAKE_IN# signal)

In case the board is plugged into a peripheral slot, it is expected that the system board controls the main power. In that case, the board boots up as soon as main power is applied.

See Table 34 in chapter 4 for information about how to configure the board for 5V standby and auto power operation.

3.6 Board Reset

The JetKit-3010 receives the reset from the CompactPCI Serial system and also controls the reset output, in case the board is used in the system slot.

The reset input and output can be configured for different behaviors.

The reset input can be received the BMC and a soft reset is performed. Alternatively, the reset can be connected to the BMC reset input so that a hard reset is performed on the BMC.

When receiving an incoming reset, the BMC also triggers the reset output in case the board is used in a system slot. It is also possible to configure the board that the reset input is automatically propagated to the reset output by hardware.

See Table 33 in chapter 4 for information on hardware configuration of the board reset.

3.7 Rear-I/O backplane support

CompactPCI Serial allows two different P6 connector options. The standard backplane provides Ethernet functionality on the P6 connector, which is supported by the Ethernet link of the JetKit-3010.

A second backplane option allows rear I/O signals from the board instead, which are received a Rear Transition Module. In case the Xavier™ board is used in such a backplane, the board can detect this and keep the Ethernet PHY in reset to keep the Ethernet lanes in high-impedance state.

See Table 33 in chapter 4 for information on how to configure the board for such a rear I/O backplane.

3.8 Board interfaces

3.8.1 USB Type C connectors

The Board houses two USB type C connectors. The pinouts can be found in Table 12 and Table 13.

Table 12 - USB-C 1 pinout

	A	B
1	GND	GND
2	USB0_TX1_P	USB0_TX2_P
3	USB0_TX1_N	USB0_TX2_N
4	VBUS_1	VBUS_1
5	USB0_CC1	USB0_CC2
6	USB0_D_P	USB0_D_P
7	USB0_D_N	USB0_D_N
8	SBU1_1	SBU2_1
9	VBUS_1	VBUS_1
10	USB0_RX2_N	USB0_RX1_N
11	USB0_RX2_P	USB0_RX1_P
12	GND	GND

Table 13 - USB-C 1 pinout

	A	B
1	GND	GND
2	USB1_TX1_P	USB1_TX2_P
3	USB1_TX1_N	USB1_TX2_N
4	VBUS_2	VBUS_2
5	USB1_CC1	USB1_CC2
6	USB1_D_P	USB1_D_P
7	USB1_D_N	USB1_D_N
8	SBU1_2	SBU2_2
9	VBUS_2	VBUS_2
10	USB1_RX2_N	USB1_RX1_N
11	USB1_RX2_P	USB1_RX1_P
12	GND	GND

The USB-C 1 connector is used to flash the NVIDIA® Xavier™. To do so, the board needs to be started in recovery mode. See chapter 0 for details.

Even though the standard Linux OS does not implement the PD controller management, the bootloader automatically sets the USB-C 1 port to device mode for programming support.

3.8.2 MicroUSB connector

The board provides one MicroUSB port with client functionality. The pinout of the MicroUSB interface can be found in Table 14.

Table 14 - MicroUSB pinout

Pin	Signal
1	MicroUSB_VBUS
2	MicroUSB_D_N
3	MicroUSB_D_P
4	-
5	GND

Attached to this port, an FTDI FT4232HQ device is connected, which provides access to four interfaces. Table 15 lists the interface types and destinations of the four ports.

Table 15 - MicroUSB interfaces

Port	Interface	Description
1	I ² C	I ² C interface to IO Expander Implementation according to Developer Kit
2	JTAG	JTAG interface to NVIDIA® Xavier™ Implementation according to Developer Kit
3	UART	UART interface to BMC
4	UART	UART interface to NVIDIA® Xavier™ Implementation according to Developer Kit

For more information regarding the UART interface, which is connected to the BMC, please see chapter 3.3.2.

3.8.3 MicroSD/UFS card slot

The board houses one MicroSD/UFS card slot. This slot can be used with normal MicroSD cards or with a high-speed UFS card. The pinout of the card slot can be found in Table 16.

Table 16 - MicroSD/UFS card slot pinout

Pin	Signal (UFS)	Pin	Signal (SD)
1	GND	13	SDCARD_D1
2	UPHY_TX10_N	14	SDCARD_D0
3	UPHY_TX10_P	15	SDCARD_CLK
4	GND	16	SDCARD_CMD
5	UPHY_RX10_N	17	SDCARD_D3
6	UPHY_RX10_P	18	SDCARD_D2
7	GND	19	GPIO2_SD_DET
8	UFS0_REF_CLK	20	GND
9	1V8_SD	21	GND
10	GPIO31_UFS_DET	22	GND
11	GND	23	GND
12	3V3_SD	24	GND
-	-	25	GND

3.8.4 Mezzanine connector

The JetKit-3010 houses an internal Mezzanine connector for custom extensions of the board functionality. The connector is Samtec QSH-060-01-L-D-A-K 120 pin high-speed socket. Pinout legend and pinout can be found in Table 17 and Table 18.

Table 17 – Mezzanine connector pinout legend

Signal Type	Signal	I / O	Description
Power	12V_SW	O	12V Switched power (SYS_VIN_HV)
	5V	O	5V Switched power (SYS_VIN_MV)
	3V3	O	3.3V power
	1V8	O	1.8V power
	GND	-	Ground
PCI Express	UPHY_5:2_TX0..3_P / N	O	PCI Express x4 Transmit differential pairs
	UPHY_5:2_RX0..3_P / N	I	PCI Express x4 Receive differential pairs
	PEX_CLK0_P / N	O	PCI Express Reference Clock output
	PEX_L0_CLKREQ_N	I	PCI Express Clock request input
	PEX_L0_RST_N	O	PCI Express reset output
	PEX0_WAKE_N	I	PCI Express wake input
	UPHY_9:8_TX0..1_P / N	O	PCI Express x2 Transmit differential pairs
	UPHY_9:8_RX0..1_P / N	I	PCI Express x2 Receive differential pairs
	PEX_CLK4_P / N	O	PCI Express Reference Clock output
	PEX_L4_CLKREQ_N	I	PCI Express Clock request input
	PEX_L4_RST_N	O	PCI Express reset output
USB	USB2_D_P/N	I / O	USB 2.0 data pair
Camera	CSI0..3_D0..1_P / N	I	CSI data pairs
	CSI0..3_CLK_P / N	I	CSI clock
	CAM0..3_MCLK	O	Camera master clock
	CAM0..1_PWDN	O	Camera power down
	CAM0..1_RST	O	Camera reset
Utility	I2C_GP3..4_CLK	O	General Purpose I ² C Clock
	I2C_GP3..4_DAT	I / O	General Purpose I ² C Data
	GPIO36_CAM_AVDD_CAM_EN	O	Camera AVDD supply enable
	GPIO25_VDD_SYS_EN	O	Camera VDD_SYS enable
	GPIO29_M2_KEYM_PEWAKE#	I	M.2 Key M PCI Express Wake input
	GPIO34_M2_KEYM_ALERT#	I	M.2 Key M PCI Alert Input

Table 18 - Mezzanine Connector pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	21	CSI2_D0_P	41	CAM0_RST	61	GND	81	UPHY_5:2_RX0_P	101	UPHY_5:2_RX3_N
2	GND	22	CSI3_D0_P	42	CAM1_MCLK	62	GND	82	UPHY_5:2_TX0_P	102	UPHY_5:2_TX3_N
3	CSI0_D0_P	23	CSI2_D0_N	43	CAM1_PWDN	63	UPHY_9:8_TX1_P	83	UPHY_5:2_RX0_N	103	GND
4	CSI1_D0_P	24	CSI3_D0_N	44	CAM2_MCLK	64	UPHY_9:8_TX0_P	84	UPHY_5:2_TX0_N	104	GND
5	CSI0_D0_N	25	GND	45	CAM1_RST	65	UPHY_9:8_TX1_N	85	GND	105	PEX_L4_CLKREQ_N
6	CSI1_D0_N	26	GND	46	CAM3_MCLK	66	UPHY_9:8_TX0_N	86	GND	106	PEX_L0_RST_N
7	GND	27	CSI2_CLK_P	47	I2C_GP3_CLK	67	GND	87	UPHY_5:2_RX1_P	107	PEX_L4_RST_N
8	GND	28	CSI3_CLK_P	48	GPIO36_CAM_AVDD_CAM_EN	68	GND	88	UPHY_5:2_TX1_P	108	PEX_L0_CLKREQ_N
9	CSI0_CLK_P	29	CSI2_CLK_N	49	I2C_GP3_DAT	69	UPHY_9:8_RX1_P	89	UPHY_5:2_RX1_N	109	PEX0_WAKE_N
10	CSI1_CLK_P	30	CSI3_CLK_N	50	GPIO25_VDD_SYS_EN	70	UPHY_9:8_RX0_P	90	UPHY_5:2_TX1_N	110	GPIO29_M2_KEYM_PEWAKE#
11	CSI0_CLK_N	31	GND	51	GND	71	UPHY_9:8_RX1_N	91	GND	111	I2C_GP4_CLK
12	CSI1_CLK_N	32	GND	52	GND	72	UPHY_9:8_RX0_N	92	GND	112	GPIO34_M2_KEYM_ALERT#
13	GND	33	CSI2_D1_P	53	1V8	73	GND	93	UPHY_5:2_RX2_P	113	I2C_GP4_DAT
14	GND	34	CSI3_D1_P	54	3V3	74	GND	94	UPHY_5:2_TX2_P	114	12V_SW
15	CSI0_D1_P	35	CSI2_D1_N	55	1V8	75	PEX_CLK4_P	95	UPHY_5:2_RX2_N	115	GND
16	CSI1_D1_P	36	CSI3_D1_N	56	3V3	76	PEX_CLK0_P	96	UPHY_5:2_TX2_N	116	12V_SW
17	CSI0_D1_N	37	GND	57	1V8	77	PEX_CLK4_N	97	GND	117	USB2_D_N
18	CSI1_D1_N	38	GND	58	3V3	78	PEX_CLK0_N	98	GND	118	12V_SW
19	GND	39	CAM0_PWDN	59	1V8	79	GND	99	UPHY_5:2_RX3_P	119	USB2_D_P
20	GND	40	CAM0_MCLK	60	3V3	80	GND	100	UPHY_5:2_TX3_P	120	5V

3.8.5 MiniHDMI connector

The JetKit-3010 houses one MiniHDMI connector to provide access to the NVIDIA® Xavier™ HDMI interface. The pinout of the MiniHDMI connector can be found in Table 19.

Table 19 - MiniHDMI pinout

Pin	Signal
1	CHASSIS
2	HDMI_D2_P
3	HDMI_D2_N
4	CHASSIS
5	HDMI_D1_P
6	HDMI_D1_N
7	CHASSIS
8	HDMI_D0_P
9	HDMI_D0_N
10	CHASSIS
11	HDMI_CLK_P
12	HDMI_CLK_N
13	GND
14	HDMI_CEC
15	HDMI_SCL
16	HDMI_SDA
17	-
18	5V_HDMI
19	HDMI_HPD

3.8.6 Ethernet connector

The JetKit-3010 houses one RJ45 connector to provide access to an Ethernet interface of the NVIDIA® Xavier™. The pinout of the RJ45 connector can be found in Table 20.

Table 20 - RJ45 pinout

Pin	Signal
1	MDI0_P
2	MDI0_N
3	MDI1_P
4	MDI2_P
5	MDI2_N
6	MDI1_N
7	MDI3_P
8	MDI3_N

Besides the Ethernet link, the RJ45 connector houses two LEDs. The indication of the two LEDs can be found in Table 21.

Table 21 - RJ45 LED indication

LED	Indication
LINK/ACT	ON – Link / BLINK – Activity
GBE	ON – Gigabit Link

3.8.7 USB2.0 connector

The JetKit-3010 houses one USB2.0 connector to provide access to a USB2.0 interface of the NVIDIA® Xavier™. The pinout of the USB2.0 connector can be found in Table 22.

Table 22 - USB2.0 pinout

Pin	Signal
1	USB2_VBUS
2	USB2_D_N
3	USB2_D_P
4	GND

3.8.8 Front Panel LEDs

The JetKit-3010 houses three green front panel LEDs as well as one red front panel LED. There is one Power LED as well as there are three user defined LEDs controlled via the NVIDIA® Xavier™. The location of the LEDs can be found in Figure 4. Information about the LEDs and control can be found in Table 23.

Table 23 - Front Panel LEDs

LED	Controlled by	Module Pin	Color	Comment
Power	SYS_VIN_HV	-	Green	Indicates Power for the Xavier™ Module
LED 1	SPARE_GPIO4	B59	Green	Lit when the module boots in non-recovery mode
LED 2	SPARE_GPIO13	G7	Green	-
LED 3	SPARE_GPIO17	A54	Red	-

The GPIO number under Linux does not correspond with the GPIO number of the signal. The GPIO number under Linux calculates from the GPIO Port, the GPIO number as well as an offset. The formula and port factors can be found in the Linux header file "tegra194-gpio.h". In the basic installation, the formula and used port factors are:

```
#define TEGRA194_MAIN_GPIO_PORT_A 0
#define TEGRA194_MAIN_GPIO_PORT_Q 16
#define TEGRA194_MAIN_GPIO_PORT_T 19
#define TEGRA194_MAIN_GPIO(port, offset) ((TEGRA194_MAIN_GPIO_PORT_##port * 8) + offset)
```

With the offset set to 288, the Linux GPIO numbers can be found in Table 24.

Table 24 - LED GPIO control

LED	Signal	Module GPIO	Linux GPIO number
LED 1	SPARE_GPIO4	GPIO3_PA.02	290
LED 2	SPARE_GPIO13	GPIO3_PT.03	443
LED 3	SPARE_GPIO17	GPIO3_PQ.01	417

3.8.9 Front Panel Push Buttons

The board houses two push buttons on the front, which are recessed to prevent pressing by mistake. The two buttons are a reset button (Reset) and a recovery button (Recov.). The location of the buttons can be found in Figure 4. Information about the buttons can be found in Table 25.

Table 25 – Push Buttons

Push Button	Signal	Module Pin
Reset	SYS_RESET_N	L60
Recov.	FORCE_RECOVERY_N	L10



To start the NVIDIA® Xavier™ in recovery mode, the recovery button needs to be pressed when the module receives power or during reset. As the BMC might be reset (see CLI command “config”), starts the bootloader first and after that powers the module, the recovery button needs to be held until the BMC provides power to the module. The moment the module receives power can be identified by the Power LED (see chapter 3.8.8).

3.8.10 BMC Programming header

The JetKit-3010 has an on-board BMC programming interface (BMC Prog). This interface is only required as a backup programming option in case the bootloader is corrupt and needs to be re-flashed.

For regular Firmware updates, please see chapter 3.3.3.

The pinout of the BMC Prog header can be found in Table 26.

Table 26 - BMC Prog pinout

Pin	Signal
1	MCLR#
2	5V
3	GND
4	ICP_PGD
5	ICP_PGC

This interface is dedicated for a Microchip PICKit 3.

Please note that an extension cable might be required to be able to plug the PICKit.



Use this programming interface only after consulting Elma. Programming requires further configuration and a specific configured bootloader file is required. This interface should not be used except cases when the bootloader gets corrupt!

3.8.11 CompactPCI Serial connectors

The JetKit-3010 has the CompactPCI Serial connectors P1, P2, P5 and P6.

The pinout of those connectors and the pinout legend can be found in the following in Table 27 to Table 31.

Table 27 - CompactPCI Serial pinout legend

Signal Type	Signal	I / O	Description
Power	12V	I	+12V main power
	5V_STDBY	I	+5V standby power
	GND	-	Ground
	NetP2_x7, NetP2_C8	I	Optional +12V power inputs (x = A, D, G, J)
CompactPCI Serial Sideband Signals	BP_I2C_SCL	I / O	I ² C System Management Bus Clock
	BP_I2C_SDA	I / O	I ² C System Management Bus Data
	PS_ON#	O	Power Supply Enable Signal
	RST_OUT#	O	Reset Output
	RST_IN#	I	Reset Input
	WAKE_IN_OUT#	I / O	WAKE# in (system Slot) / out (periph. Slot)
	SYSEN#	I	System / Peripheral Slot indicator
	GA0_PWRBTN#	I	Power Button (system Slot) / GA0 (periph. Slot)
	GA1_PWRFAIL#	I	Power Fail (system Slot) / GA1 (periph. Slot)
	GA2	I	Geographic Address Input 2
	GA3	I	Geographic Address Input 3
	DECT_BPR	I	Detect Backplane Routing
	DECT_RIO	I	Detect Rear I/O
PCI Express	NVHS0_TX0..7_P / N	O	PCI Express Transmit differential pairs
	NVHS0_RX0..7_P / N	I	PCI Express Receive differential pairs
	NVHS0_REFCLK0_P / N	I	PCI Express Reference Clock input
	PEX_CLK5_P / N	O	PCI Express Reference Clock output
	PCIE_EN#	O	PCI Express Clock Request output
	CLKREQ_IN#	I	PCI Express Clock Request input
USB	1_USB3_TX_P / N	O	USB3 Transmit differential pair
	1_USB3_RX_P / N	I	USB3 Receive differential pair
	1_USB2_P / N	I / O	USB2 data pair (bidirectional)
Ethernet	1_ETH_A..D_P / N	I / O	Gigabit Ethernet differential pairs (bidirectional)

Table 28 - P1 CompactPCI Serial connector

	L	K	J	I	H	G	F	E	D	C	B	A
6	NVHS0_RX3_N	NVHS0_RX3_P	GND	NVHS0_TX3_N	NVHS0_TX3_P	GND	NVHS0_RX2_N	NVHS0_RX2_P	GND	NVHS0_TX2_N	NVHS0_TX2_P	GND
5	GND	NVHS0_RX1_N	NVHS0_RX1_P	GND	NVHS0_TX1_N	NVHS0_TX1_P	GND	NVHS0_RX0_N	NVHS0_RX0_P	GND	NVHS0_TX0_N	NVHS0_TX0_P
4	-	-	GND	-	-	GND	NVHS0_REFCLK0_N	NVHS0_REFCLK0_P	GND	1_USB2_N	1_USB2_P	GND
3	GA3	-	-	GA2	-	-	GA1_PWRFAIL#	1_USB3_RX_N	1_USB3_RX_P	GA0_PWRBTN#	1_USB3_TX_N	1_USB3_TX_P
2	SYSEN#	PCIE_EN#	GND	WAKE_IN_OUT#	RST_IN#	GND	RST_OUT#	PS_ON#	GND	BP_I2C_SDA	BP_I2C_SCL	GND
1	GND	12V	12V	GND	12V	12V	GND	12V	12V	GND	5V_STDBY	12V

Table 29 – P2 CompactPCI Serial connector

	L	K	J	I	H	G	F	E	D	C	B	A
8	-	-	-	-	-	GND	-	-	GND	NetP2_C8	-	GND
7	GND	-	NetP2_J7	GND	-	NetP2_G7	GND	-	NetP2_D7	GND	-	NetP2_A7
6	-	-	GND	-	-	GND	-	-	GND	-	-	GND
5	GND	-	-	GND	-	-	GND	-	-	GND	-	-
4	-	-	GND	-	-	GND	-	-	GND	-	-	GND
3	GND	-	-	GND	-	-	GND	-	-	GND	-	-
2	NVHS0_RX7_N	NVHS0_RX7_P	GND	NVHS0_TX7_N	NVHS0_TX7_P	GND	NVHS0_RX6_N	NVHS0_RX6_P	GND	NVHS0_TX6_N	NVHS0_TX6_P	GND
1	GND	NVHS0_RX5_N	NVHS0_RX5_P	GND	NVHS0_TX5_N	NVHS0_TX5_P	GND	NVHS0_RX4_N	NVHS0_RX4_P	GND	NVHS0_TX4_N	NVHS0_TX4_P

Table 30 – P5 CompactPCI Serial connector

	L	K	J	I	H	G	F	E	D	C	B	A
6	-	-	-	-	-	-	-	-	-	-	-	-
5	-	-	-	-	-	-	-	-	-	CLKREQ_IN#	PEX_CLK5_N	PEX_CLK5_P
4	-	-	GND	-	-	GND	-	-	GND	-	-	GND
3	GND	-	-	GND	-	-	GND	-	-	GND	-	-
2	-	-	GND	-	-	GND	-	-	GND	-	-	GND
1	GND	-	-	GND	-	-	GND	-	-	GND	-	-

Table 31 – P6 CompactPCI Serial connector

	L	K	J	I	H	G	F	E	D	C	B	A
8	-	-	GND	-	-	GND	-	-	DECT_BPR	-	-	DECT_RIO
7	GND	-	-	GND	-	-	GND	-	-	GND	-	-
6	-	-	GND	-	-	GND	-	-	GND	-	-	GND
5	GND	-	-	GND	-	-	GND	-	-	GND	-	-
4	-	-	GND	-	-	GND	-	-	GND	-	-	GND
3	GND	-	-	GND	-	-	GND	-	-	GND	-	-
2	-	-	GND	-	-	GND	-	-	GND	-	-	GND
1	GND	1_ETH_D_N	1_ETH_D_P	GND	1_ETH_C_N	1_ETH_C_P	GND	1_ETH_B_N	1_ETH_B_P	GND	1_ETH_A_N	1_ETH_A_P

4 Configuration

The board houses three 4 pole DIP switches as it can be seen in Figure 16.

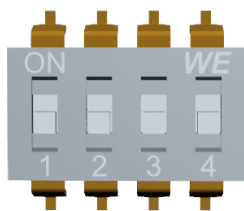


Figure 16 - 4 pole DIP switch

The switch is active, when the switch is slid to the "ON" side of the housing.

Table 32 to Table 34 list the switch functionalities of the switches SW3, SW5 and SW6. Default configurations are highlighted in light blue color.

Table 32 - DIP Switch SW3 Functionality

Switch	Setting	
1	OFF	No automatic CLKREQ# input when board is in a system slot
	ON	CLKREQ# is automatically set as input when board is in a system slot
2	OFF	No automatic CLKREQ# output when board is in a peripheral slot
	ON	CLKREQ# is automatically set as output when board is in a peripheral slot
3	OFF	No manual configuration of CLKREQ# input
	ON	CLKREQ# is set as input
4	OFF	No manual configuration of CLKREQ# output
	ON	CLKREQ# is set as output

Table 33 - DIP Switch SW5 Functionality

Switch	Setting	
1	OFF	BMC programming mode (BMC reset connection)
	ON	BMC run mode (normal operation)
2	OFF	Perform BMC soft reset when receiving reset input
	ON	Perform BMC hard reset when receiving reset input
3	OFF	No hardware reset in to out propagation
	ON	Hardware reset in to out propagation
4	OFF	Ethernet PHY always on
	ON	Keep Ethernet PHY in reset when plugged in a rear I/O backplane

Table 34 - DIP Switch SW6 Functionality

Switch	Setting	
1	OFF	No auto power (wait for power button or wake input)
	ON	Auto power (only when operation from 5V standby is permitted)
2	OFF	Run from main power only
	ON	Run from main power or from 5V standby
3	OFF	BMC programming mode (BMC programming clock connection)
	ON	BMC UART to Quad UART connection (normal operation)
4	OFF	BMC programming mode (BMC programming data connection)
	ON	BMC UART to Quad UART connection (normal operation)

5 Mezzanines

The mezzanine interface connector (see chapter 3.8.4) provides a variety of signals, which can be used to expand the functionality of the board and further interfaces to the board.

The interfaces available on the mezzanine connector are:

- PCI Express x4
- PCI Express x2
- USB2.0
- 4x CSI camera interfaces
- Utility signals (camera enable signals, M.2 type M sideband signals)

The standard mezzanine of the JetKit-3010 houses an M.2 2242 socket, an Ethernet NIC and a USB2.0 interface connector. Details of the standard mezzanine can be found in chapter 2.5.5.

Custom mezzanine boards can be designed based on the interfaces available on the mezzanine connector.



Contact Elma when a custom mezzanine is required for your application.

6 Ordering Information

Table 35 - Ordering Information

ELMA PN	Description
066-594	<u>JetKit-3010</u> CompactPCI Serial NVIDIA® AGX Xavier™ board with Nvidia Industrial module, 3U / 8HP FP I/F: 2x USB-C, MicroUSB, USB2.0 Type A, MiniHDMI, 1000Base-T on RJ45, MicroSD/UFS BP I/F: PCIe x8, 1000Base-T, USB3.1

7 Technical Support

7.1 Contact

For technical assistance, please contact us via:

E-mail: support@elma.de or
Web: <http://www.elma.de>
Telephone: +49 7231/9734-0

Please take care that your request contains the following information:

- System / Product part number
- System / Product serial number, can be found on the type label on the inner right sidewall or on the board connector or PCB.
- A short description of the faulty behavior of your system

7.2 Returning Defective Products

Please follow these steps before you return any faulty systems or accessory to ELMA Electronic GmbH:

1. Please contact the ELMA Electronic GmbH RMA team to receive the RMA form via rma@elma.de
2. After receiving the RMA form via e-mail, please fill the form and send it back to the RMA team.
3. Please take care to provide us the name, telephone number and e-mail address of a person we can contract to obtain more information if necessary.
4. Describe the fault of your system or accessory (as detailed as possible).
5. When returning a system or accessory please take care of the following points:
 - Pack it securely in its original packaging (if still available)
 - Enclose a copy of the RMA form with your delivery note

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